PATENT ABSTRACTS OF JAPAN

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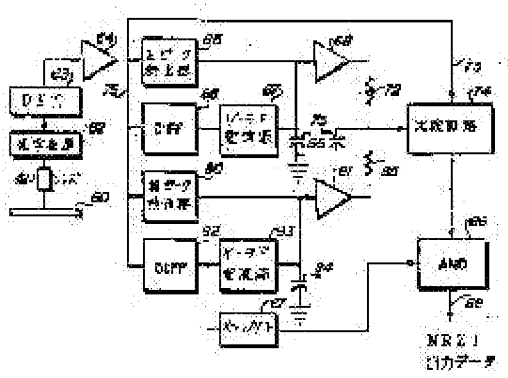
(54) DEVICE AND METHOD FOR DETECTING DIGITAL DATA SIGNAL

(57)Abstract:
PURPOSE: To cope with a base line shift of an input signal waveform and to perform transition detection without noise.

CONSTITUTION: A data detecting circuit is provided which adopts one of technologies for an amplitude and a transition position so as to adjust a detection threshold for a following shift on the base line of a signal to be detected. In case of the amplitude technology, an intermediate amplitude value between a series of positive and negative detected peaks is held in an averaging capacitor 73, threshold adjustment is performed in a single detection period, and the detection threshold is adjusted so that it can be used in a following detection period. A zero axis crossing of an analog signal is detected with a tracking detection threshold and an NRZI digital waveform is generated by an analog AND circuit 81. For transition position detection, a series of temporal relative positions of transition represented by the sampling of the transition of a read signal is integrated and averaged to perform detection for tracking the base line shift.



CLAIMS

[Claim(s)]
[Claim 1]A device which detects a digital data signal, comprising:
A means to receive a data signal which carries digital information which should be detected.
A means to differentiate a received data signal and to supply a this differentiated signal.
A peak circuit means which provides a sampling aperture which is in agreement with transition in a data signal which received said differentiated signal, detected a peak positive [the] and negative and was received to each detected peak.
It is connected to said means to receive, and receive said received data signal, and it is connected to said peak circuit means, and each sampling aperture signal is answered, A sample hold circuit means to sample a current value at that time of a data signal been [a data signal / it] late and received as a value which directs a baseline, and to memorize it, A detector circuit means to detect a value of data which used said baseline which shows a value for 0 axis intersection which shows transition which it is connected to said sample hold circuit means, and is generated in the next of a received data signal, and was directed by a received data signal.

[Claim 2]A device which detects the digital data signal according to claim 1 containing an equalization means by which said sample hold circuit means equalizes a series of values of a different polar transition sample.
[Claim 3]Detect a REBERURU shift of DC baseline of said data signal, and detection threshold level shifted with said baseline is set, How to detect a data signal containing a step which carries out amplitude detection of the data signal using said detection threshold level to data transition which continues also in said data signal.
[Claim 4]Measure one of the peak amplitude of said data signal, and one peak amplitude next to said data signal which has signal polarity opposite to the one aforementioned peak amplitude next is measured, A method according to claim 3 of containing further a step which generates said detection threshold level by equalizing two values of the measured aforementioned peak amplitude.
[Claim 5]Differentiate said data signal, and this differentiated signal peak amplitude exceeds positive predetermined amplitude threshold level, or negative predetermined amplitude threshold level only at the time of lower ****. A method according to claim 4 of containing further a step which detects said baseline level shift by detecting a peak of a differentiated this signal.
[Claim 6]In a device which detects transition in a data signal which has between patent periods which can detect data, A single envelope of a data signal is analyzed between each patent periods of a signal, Next, 1st means to set up amplitude detection threshold level which has a

predetermined amplitude relation to a signal envelope as which the above was analyzed to between patent periods to generate, A device which detects transition of a data signal containing the 2nd means that carries out the magnitude comparison of said data signal and said amplitude detection threshold level between patent periods generated in the next of a data signal.
[Claim 7]Between each patent period, said data signal has two or more peak amplitude, and it said 1st means, The device according to claim 6 which contains further a peak detection means to detect amplitude of two opposite peaks, and an equalization means to equalize peak amplitude which was connected to said peak detection means and detected, and to supply the aforementioned average as said amplitude detection threshold level.
[Claim 8]The device according to claim 7 which said 1st means has a differential means which differentiates said data signal, and said peak detection means is combined with said differential means, and carries out peak detection of the amplitude of two peaks of the differentiated aforementioned data signal.
[Claim 9]A gate means connected to said 2nd means in order to receive the detected aforementioned data signal, The device according to claim 6 which contains further a gap means which lets a data signal detected only when said data signal was received, and said gate means was energized and said genuine signal was directed, in order to direct a time of a genuine data signal being received pass.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application]About a data detector, it is usable with Pulse Density Modulation (PWM), and especially this invention relates to the detector used with an optical disk recorder.
[0002]
[Description of the Prior Art]When digital one or a bipolar signal becomes out of balance toward the polarity of one side or another side, digital one or digitized signal processing is always easy to be influenced to the baseline shift of a signal, and the shift which goes to superior polarity turns a baseline to the polarity, and is moved.
[0003]The baseline shift of a digital waveform (known also as a binary signal) like the NRZI pattern 16 shown in drawing 1 is not carried out at all, but this only means being that there are two levels in the waveform. A waveform has the transition parts between a high level which **** by HI, the low directed by LO, and two levels directed by T. Ideal reproduction of a digital waveform requires a straight-line analog channel with an infinite band belt without a noise.
[0004]Distortion is experienced when a digital waveform passes along an analog channel like magnetic tape writing / read channel, or optical disc writing / read channel. Distortion is produced when a noise is added, that the band belt of a channel is mainly restricted, and. As for a high-frequency (that is, wavelength is short) signal, amplitude becomes small from a low frequency (that is, wavelength is long) signal, the high-frequency limit, i.e., the high-frequency roll-off, of a channel. The waveform 18, i.e., a signal, shows the roll-off distortion of high frequency. The AC couplings adopted in the channel in order to eliminate the DC shifts and the drift between the stages of the versatility of a digital disposal circuit remove the DC component of a signal, therefore a baseline shift. A baseline is an ideal line which connects the average mark between the peaks of two opposite hands where an analog-spectrum form adjoins. The reference number 19 shows a baseline shift. According to wavelength and a digital sequence, an analog

signal shifts the baseline with the both sides of a high-frequency roll-off and AC cup rig. Another causes by which the baseline of the rereading signal in an optical disc channel moves are the medium reflectance of an optical disk substrate, and change of a double reflex. It is difficult to generate the peak of an analog-spectrum form, and transition for the above-mentioned reason in the level which versatility cannot predict frequently, and to detect with sufficient reliability in the detector of the conventional threshold level immobilization.

[0005]In a data detector, a baseline shift may shift a transition position seemingly (shift of the 0 axis intersection accompanying a baseline shift). On the other hand, law is providing the balanced code which permits or prevents a baseline shift also a little. That is, the quantity of one polar signal is equal to the same quantity of the polar signal of another side, therefore it is making it the DC component of the net of a signal serve as zero. For this reason, it is desirable to provide the data detection system with which one in increase, therefore a signal baseline of DC shifts also compensates the overhead of the recorded data promptly.

[0006]The simplest method of detecting the analog-data transition which carries digital information is comparing an analog-data wave amplitude with the threshold level of fixed amplitude, for example. In such detection, whenever the amplitude of an analog signal crosses threshold level, transition is shown. The inclination of analog transition, i.e., the inclination of a 0 axis intersection, changes by many factors containing a reading channel bandwidth and its characteristic. Generally, an inclination is smaller as a bandwidth is small. As an inclination is small, when detecting the signal by which Pulse Density Modulation was carried out, it is more difficult to acquire the exact position of required 0 axis intersection. It is common knowledge that the analog signal baseline (DC levels) is always moving. The actual crossing between a transition part and fixed threshold level shifts, and a data detection error is generated. If an analog signal moves the upper part or a lower part thoroughly [fixed threshold level], detection of transition cannot be performed well. By baseline movement of the optical disc of a rereading signal returned to an analog signal. It changes by the double reflex of the substrate with which it shifts toward one of polarity for exchange (AC) coupling used frequently, and changes dynamically, and reads with the reflectance of a medium, namely, a detection laser beam reaches the recording layer of an optical medium through there.

[0007]The general transition detecting method for the above-mentioned baseline shift is the method of carrying out peak detection of the signal which differentiated the received analog signal and then was differentiated. The differentiated signal is re-differentiated in many cases, in order to obtain 0 axis intersection, and 0 axis intersection is in agreement with each peak of the differentiated signal in time. Two 0 axis intersections are detected by detecting these 0 axis intersections. The problem concerning differentiation detection is the increase in the noise which accompanies a differentiation process. Of course, by differentiation, the high-frequency response in a read channel is increased, and a high frequency noise is raised. Theoretically, reduction of a signal-noise ratio is about 6 decibels. It is desirable to eliminate the aforementioned problem and to make a baseline shift reduce the sensitivity to a baseline with the application of this detection system.

[0008]The differentiation of a reading signal is used again, also in order to detect at the time of **. That is, the zero crossing of the differentiated signal is in agreement with the peak of a reading signal in time. U.S. Pat. No. 4,475,183 besides Marchant (Marchant et al) shows such a system. This system is also influenced by the phase shift of the transition position in the detection process which should be eliminated.

[0009]U.S. Pat. No. 4,418,406 to Ogawa (Ogawa) shows the signal wave control circuit which

has the 2nd input side to the comparator for receiving an input signal, and the comparator for receiving a reference level signal. An output terminal conveys the output signal which has positive [corresponding to an input signal], and a negative portion. A detector detects the greatest or minimum transition interval included in an output signal in order to generate a detected signal. A hold circuit holds a detected signal, and when a control circuit generates a reference level signal, it is made for the interval of the positive portion of an output signal and the interval of the negative portion of an output signal to become equal. Therefore, said circuit is a system which eliminates the shift of DC-baseline, and an operation of an analog signal. This circuit needs the limited code system with which the run length which increases the record overhead of the data recorded as mentioned above was balanced. Therefore, a baseline regulation system with much more pliability more than what is shown in said Ogawa's patent is desired.
[0010]
[Problem(s) to be Solved by the Invention]The purpose of this invention is to provide DC baseline compensation which improved.
[0011]Another purpose of this invention is to provide the transition detection which detects transition, without paying the compensation of conquering the baseline shift in an input signal waveform, and increasing a noise.
[0012]
[Means for Solving the Problem]A baseline tracking threshold level detector by this invention pursues a motion of a baseline of an input data signal. A baseline shift is generated by being extracted from a rereading signal, i.e., an input signal, and sampling an input signal which tracking threshold level should detect, and adjusting detection threshold level as a baseline shift in data detection time.
[0013]In one aspect of affairs of this invention, a baseline position at the time of one detection, i.e., a sampling, holds a value of DC baseline detection threshold level till the next sampling. As for a sampling of an input data signal, it is preferred to attain by detecting a peak of an input analog signal, i.e., the point of inflection of transition.
[0014]In an example with this invention, a positive and negative peak detector specifies a peak envelope of a rereading signal, i.e., an analog signal, which should be detected. A peak value is equalized in order to find out detection threshold level. Subsequently, a tracking baseline is used as a standard which detects transition in specified sampling time.
[0015]In another example of this invention, a base line value is equalized among a series of transition position fields using the above-mentioned peak value equalization. In a specific form of this invention, a signal which should be detected is overdue by between [1 time of] patent periods. DC baseline tracking occurs between delay between 1 time of this patent period. In the end of the delay, amplitude of data in a signal to which tracking threshold level to an overdue signal was received and which was in it is detected correctly.
[0016]The above-mentioned of this invention and the other purposes, the feature, and an advantage become clear from the following explanation about a preferred embodiment of this invention shown in an accompanying drawing.
[0017]
[Example]Refer to the accompanying drawing which directs the same member that has a structural feature for the same number below in the figure of ****. The portion 10 of an optical disc shows the track which has the track center line 15 which was recorded and was provided with the photodetection nature spots 11, 12, 13, and 14. The spot 11-14 can be detected in magneto-optics on a magneto-optics medium, or can perform detection of intensity modulation,

for example like ablation medium (ablative) and phase change medium. The recorded spot 11-14 is in the flat face of said portion 10. That is, in this specific example, although the slot is not shown, it is understood that an optical medium with flatness or a slot can be adopted. This principle can be used also to the magnetic recording of a certain kind of type. In order to record the spot 11-14 showing the transition data 17, the record signal 16 is used. In this transition data 17, the binary 1 shows the transition in a transition position, and, on the other hand, binary zero show not being placed between the transition positions along the track 15 by transition. The information recorded on the mark 11-14 is drawn from the pulse temporal duration in the record signal 16, i.e., the space between a series of transition, and provides the signal by which Pulse Density Modulation was carried out. Being able to apply the principle of this invention to pulse phase modulation, each of the positive peak position provided with the data 17 directs the only information as everyone knows to pulse position modulation. The reading signal 18 is acquired by detecting the information recorded on said portion 10. 1/2 wave with two long continuation shown for [11 and 12] the recorded wave-like imbalance (i.e., spots) shifts the DC baseline 19 of a rereading signal. According to this invention, the shift of the DC baseline 19 is adjusted in each of the transition position which the binary 1 in the data 17 shows.

[0018]Drawing 2 shows the conventional technology which the DC baseline 19 reads over also as a shift and carries out amplitude detection of the signal 18. He should understand that a possibility of a noise reading over, and it being introduced into a channel, and data losing, or acquiring error data is comparatively high. Generally, these systems are constituted to low density record, respectively. The noise produced by the rise of high frequency can introduce an error in a data detection process. Have often been called the jitter as shown in the parenthesis 33 which shows the variability region of the transition parts which were produced by the noise shown by the hash mark 34 of the signal 30, and which are not meant by this shift. According to one aspect of affairs of conventional technology, reading signal R reproduces the differential signal 25 which differentiates and has the fixed (dR/dt) baseline 26. The differentiated signal 25 acquires the signal 30 (dR'/dt) which differentiates again and has the baseline 31. Using 0 axis intersection of the signal 30, detection of the peak of the signal 25 is carried out at the time of **, and the data out signal 32 by which shaping detection was carried out is generated. It is necessary to remove the zero crossing which the signal 30 mistook by detecting the low amplitude portion of the signal 25, for example.

[0019]Drawing 3 shows 1 set of signal wave forms in which the principle which derives detection tracking amplitude threshold level, for example from an amplitude sample like the peak amplitude of the rereading signal 18 is shown. A detection process generates the positive signal envelope 40 and the negative signal envelope 41, and each envelope actually relates to the peak amplitude value positive [of the rereading signal 18 / each], and negative. The detection threshold level 42 pursues DC unbalanced shift of the baseline 19 by equalizing the value of the envelope signals 40 and 41 shifted with DC baseline. The reading signal 18 differentiates and the differential signal 25 is generated. Zero axes of the reading signal 18, i.e., baseline intersection, are in agreement with the signal 25 which differentiated peak amplitude in time. If there is peak amplitude of the differential signal 25 which is a peak of lower ******, the output pulses 43 and 44 will generate a peak and the threshold level 46 positive [exceeding the threshold level 45]. These pulses carry out the gate of 83 for the current source 67 into the temporal duration of positive [of the differential signal 25], and a negative pulse in order to make the storage capacitors 69 and 84 discharge. These capacitors memorize positive [which were received from the detectors 65 and 80, respectively], and a negative signal peak value, respectively. Discharge

of each capacitor is generated just before detecting the following peak. By this discharge, tracking of a lower peak value is made possible (the amplitude of the signal peak of small amplitude is shown faithfully). When that is not right, the storage capacitors 69 and 84 can continue memorizing the peak value of high amplitude rather than preceding. The detected NRZI signal 32 is generated by detecting the signal 18 which crosses the baseline 42.

[0020]The value 42 of DC baseline, i.e., a detection tracking baseline, is held between 0 axis intersections of the reading signal 18. In zero axis each intersection of the reading signal 18, a baseline is measured again and detection threshold level is adjusted. Therefore, since this amplitude drawn from the DC baseline 42 is thoroughly adjusted in each of 0 axis intersection of the reading signal 18, it pursues the shift of the baseline of the reading signal 18 promptly. This adjustment is generated twice to each of one perfect cycle of the reading signal 18. For example, in drawing 3, the 1st baseline adjustment draws a curve by the comparison 42A of the peak amplitude of the reading signals 40A and 41A. The 2nd adjustment in 42B shows the shift from the detection threshold level tracking level 42 of drawing 3 to the **** upper part. This adjustment is performed by measuring the amplitude difference between the peaks 40B and 41B. Small adjustment of 42A-1 which is adjustment is attained by the right peak detector 65 which acquires the positive peak 40B. This alignment procedure is repeated during signal processing of the rereading signal 18. The negative peaks 41A, 41B, and 41C are carried out in this way, and are pursued by the negative peak detector 80.

[0021]In this invention, 0 axis intersection of the reading signal 18 and the detection threshold level which pursues the baseline 42 equalize the amplitude of the peaks 40A and 41A. Therefore, it can be made to generate.

The equalizing circuit comprises the positive envelope buffer 68, the resistance 72, the negative envelope buffer 81, the resistance 85, and the equalization capacitor 73.

[0022]The transition which follows baseline measurement immediately is used in the 1st example. In the 2nd example, the transition located in the middle to the peak amplitude of the contiguity used in order to generate the corrected baseline detection threshold level is used. As for detection of data, and adjustment of a baseline, the detection threshold level 42, i.e., the baseline made to adjust, follows a shift and amplitude value of a rereading signal promptly very dynamically therefore. The signal wave form of the lot which can be used in order that drawing 4 may explain drawing 6 is shown, and tracking threshold level follows the baseline to shift based on the sampling of transition. This system is dynamic just like the thing explaining drawing 3, and is a preferred embodiment of present this invention. In this system, the rereading signal 18 is analyzed, makes the tracking threshold level 50 generate, and shifts this threshold level 50 with the shift of a baseline. The amplitude threshold level 52 and 53 of a lot detects the peak of the differential signal 25, and identifies 0 axis intersection of the reading signal 18. These values are adjusted in zero axis each intersection of the rereading signal 18. The reference numbers 54 and 55 show the sample of downward transition and the sample of rise transition in the signal 18, respectively, and they are sampled and equalized and derive detection threshold level.

[0023]After sampling and equalizing each denture (denture), it is made to memorize by the sample hold circuit mentioned later. This sample hold circuit holds the level of the drawn tracking threshold level 50. The signals 57 are positive [of the differentiated signal 25], and a group of the unipolar signal corresponding to the sampling aperture of negative transition. The NRZI rereading data signal 32 is generated by detecting the signal 18 which crosses the threshold level 50. Drawing 6 and drawing 7 show the detector circuit using the data detection art shown in drawing 4 which performs dynamic baseline shift adjustment.

[0024]Next, if drawing 5 is referred to, the optical disc 60 whose portion of 10 is a part of 3 will be detected in the usual way by the lens 61 and the optical apparatus 62 which can exercise using laser (not shown) so that focusing is possible. Relative focusing and positioning of the optical lens 61 to the optical disc 60 are common knowledge, therefore it is not explaining. Either of the optical apparatuses used for magneto-optics signal detection, phase change signal detection, etc. may be sufficient as the optical apparatus 62. To all the recording systems, the suitable reading signal detector 63 detects the recorded data, and supplies the signal 18 to the read amplifier 64, and this amplifier 64 supplies the amplified signal to the illustrated detector circuit.
[0025]The positive envelope signal 40 is generated by the circuit containing the right peak detector 65. This detector 65 supplies that positive peak detection signal to the operational amplifier 68. The capacitor 69 holds the peak value detected until the next transition was detected. If the next transition is detected, the differentiator 66 will generate the signal 25 from the rereading signal 18, and will be supplied to the GETEDO current source 67. If the signal 25 exceeds the positive threshold level 45, the GETEDO current source 67 will answer the positive peak of the differential signal 25, and will discharge the capacitor 69 promptly. If the storage capacitor 69 is discharged selectively, the right peak detector 65 will be charged at urgency to a new peak value as shows the capacitor 69 by 40B of drawing 3. Subsequently, the detected aforementioned value is held until it generates, as positive 0 axis intersection of the following shows by 40C of drawing 3. The operational amplifier 68 supplies the sample hold value memorized by the capacitor 69 to the resistance equalizing circuit containing the resistance 72 and 85 and the smoothing capacitor 73. The value held by the smoothing capacitor 73 is average value showing the detection tracking signal 42.
[0026]The negative peak envelope 41 is generated including the negative peak detector 80 by the circuit which supplies the value to the operational amplifier 81 and the storage capacitor 84. The same with having mentioned above about the positive peak, the capacitor 84 holds the value of the negative peak to the input side of the operational amplifier 81 until transition negative [next to the reading signal 18] is detected. That is, this signal is held until it comes to have the negative peak amplitude in which the signal 25 is lower than the amplitude threshold level 46. The differentiator 82 differentiates the signal 18 again and supplies the differentiated signal to the GETEDO current source 83. The GETEDO current source 83 answers the lower **** signal 25 in the negative threshold level 46, and discharges the capacitor 84 promptly. After the storage capacitor 84 is discharged selectively, in the negative peak value which charged the capacitor 84 promptly and from which the reading signal 18 was detected exactly, the negative peak detector 80 resets up the negative envelope value 41. The operational amplifier 81 supplies the signal 41 to the capacitor 73 via the resistance 85. It has impedance with the equal resistance 72 and 85, therefore the mean value between two peaks, positive [which was detected continuously] and negative, is found out, and the signal 42 is generated.
[0027]Data detection is attained by three elements shown in drawing 5. In order that a comparison circuit may compare with the signal 42, the signal 18 is received via the line 75. The NRZI signal from this comparison is supplied to analog circuitry AND86, and analog circuitry AND86 is energized and generates a series of pulses which show the NRZI data output shown as the signal 32 in drawing 3 on the line 88. Only when the data signal is detected, AND86 enables it for the gap gate 87 to let the digital signal 32 pass from the comparator 74 to the line 88. Positive [of exceeding or the lower **** signal 25] and a negative peak generate the pulses 43 and 44 for the positive and negative thresholds 45 and 46, respectively. Since the gap gating function 87 is produced, the pulses 43 and 44 are used. The gap gate 87 answers the signal 25

supplied by the differentiator 82, and directs when an authentic data signal is received. In many records, it is between the blocks with which the signal was recorded, a gap, i.e., a field, without a signal. The gap gate 87 detects the block of such a gap or a signal in a well-known way, for example according to envelope detection, integration, etc. The gap gate 87 carries out the gate of the signal 32 detected from the comparator via the AND date 86.

[0028]Drawing 6 shows the circuit which performs the transition position detection phase of this invention. The operational amplifier 64 supplies the amplified rereading signal 18 to the comparison circuit 90 via the line 91. The rereading signal 18 is supplied to sample hold circuit S&H 92, and as this circuit 92 was started and drawing 4 was explained, it samples a signal again. The differentiator 94 generates the signal 25, and this signal exceeded the threshold level 52, or makes the sample gate 95 it to be compared with the amplitude threshold level 52 and 53, and energize the threshold level 53 to an amplitude working range positive [of the lower ****** signal 25], and negative about this point. A series of two integration with the sample hold amplitude 54 and 55 is supplied to the integrating capacitor 93, and supplies the signal 50 to the comparison circuit 90. The integration of the signal in the capacitor 93 is the integration of time and amplitude, and gives directions of transition. As for the capacitor 93, it is large enough to it being few and making it make that the detection threshold level 50 shifts more nearly dynamically than the threshold level 42. The NRZI pulse 32 occurs by the result of the comparison 90 between the reading signal 18 and the threshold level 50.

[0029]Drawing 7 shows the circuit which detects 0 axis intersection of the signal 18. The line 75 carries the signal of the operational amplifier 64 to the differentiator 100, and this differentiator 100 generates the signal 25 (drawing 4). The signal 25 follows even the peak amplitude comparison detection machines 101 and 102 of a couple. The comparator 101 has the reference value supplied by the potentiometer 103, and generates the voltage threshold level 52. The comparator 101 supplies the fixed amplitude signal which is sampled in the circuit 110, is held and is equalized to OR gate 105. Similarly, to the negative working range of the differentiated signal 25, the potentiometer 104 supplies the voltage threshold level 53, and this threshold level 53 is supplied to the reference input side of the switching comparator 102. the signal 25 -- the threshold level 53 -- lower ****** -- a gating signal is supplied to OR circuit 105, and it lets when pass to a sample, equalization, and the hold circuit 110. Gating pulses are the same temporal duration and the same amplitude.

Therefore, these signals should note reading over in contrast with the peak amplitude used to the example shown in drawing 5, and expressing a transition position.

[0030]Drawing 8 shows the suitable structure of the sample, equalization, and hold circuit which is publicly known composition. The signal of the line 113 is supplied as an input to the switching amplifier 120. The peak indication signal on the line 106 supplied by OR circuit 105 makes the charge pump 120 one, samples the amplitude of the signal 18, and compares it with the current value of the detection threshold level signal 50 on the line 112. The amplitude difference detected by the circuit 120 between an input value and a reference current value adjusts the voltage memorized by the capacitor 121 into the temporal duration of the peak instruction pulse 57. The memorized value continues being supplied to the operational amplifier 122, and this amplifier 122 supplies the tracking detection threshold level signal 50 on the line 112. The sample, equalization and hold-circuit S&H 92 of drawing 6, and the capacitor 93 are substituted for the circuit shown in drawing 8.

[0031]Although this invention has been illustrated and explained especially with reference to a

preferred embodiment, in a gestalt and details, what can be changed is understood variously, without deviating from the pneuma and the range of this invention to the specialist in the technical field concerned.

TECHNICAL FIELD

[Industrial Application]About a data detector, it is usable with Pulse Density Modulation (PWM), and especially this invention relates to the detector used with an optical disk recorder.

PRIOR ART

[Description of the Prior Art]When digital one or a bipolar signal becomes out of balance toward the polarity of one side or another side, digital one or digitized signal processing is always easy to be influenced to the baseline shift of a signal, and the shift which goes to superior polarity turns a baseline to the polarity, and is moved.
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[0005]In a data detector, a baseline shift may shift a transition position seemingly (shift of the 0 axis intersection accompanying a baseline shift). On the other hand, law is providing the balanced code which permits or prevents a baseline shift also a little. That is, the quantity of one polar signal is equal to the same quantity of the polar signal of another side, therefore it is making it the DC component of the net of a signal serve as zero. For this reason, it is desirable to provide the data detection system with which one in increase, therefore a signal baseline of DC shifts also compensates the overhead of the recorded data promptly.
[0006]The simplest method of detecting the analog-data transition which carries digital information is comparing an analog-data wave amplitude with the threshold level of fixed

amplitude, for example. In such detection, whenever the amplitude of an analog signal crosses threshold level, transition is shown. The inclination of analog transition, i.e., the inclination of a 0 axis intersection, changes by many factors containing a reading channel bandwidth and its characteristic. Generally, an inclination is smaller as a bandwidth is small. As an inclination is small, when detecting the signal by which Pulse Density Modulation was carried out, it is more difficult to acquire the exact position of required 0 axis intersection. It is common knowledge that the analog signal baseline (DC levels) is always moving. The actual crossing between a transition part and fixed threshold level shifts, and a data detection error is generated. If an analog signal moves the upper part or a lower part thoroughly [fixed threshold level], detection of transition cannot be performed well. By baseline movement of the optical disc of a rereading signal returned to an analog signal. It changes by the double reflex of the substrate with which it shifts toward one of polarity for exchange (AC) coupling used frequently, and changes dynamically, and reads with the reflectance of a medium, namely, a detection laser beam reaches the recording layer of an optical medium through there.

[0007]The general transition detecting method for the above-mentioned baseline shift is the method of carrying out peak detection of the signal which differentiated the received analog signal and then was differentiated. The differentiated signal is re-differentiated in many cases, in order to obtain 0 axis intersection, and 0 axis intersection is in agreement with each peak of the differentiated signal in time. Two 0 axis intersections are detected by detecting these 0 axis intersections. The problem concerning differentiation detection is the increase in the noise which accompanies a differentiation process. Of course, by differentiation, the high-frequency response in a read channel is increased, and a high frequency noise is raised. Theoretically, reduction of a signal-noise ratio is about 6 decibels. It is desirable to eliminate the aforementioned problem and to make a baseline shift reduce the sensitivity to a baseline with the application of this detection system.

[0008]The differentiation of a reading signal is used again, also in order to detect at the time of **. That is, the zero crossing of the differentiated signal is in agreement with the peak of a reading signal in time. U.S. Pat. No. 4,475,183 besides Marchant (Marchant et al) shows such a system. This system is also influenced by the phase shift of the transition position in the detection process which should be eliminated.

[0009]U.S. Pat. No. 4,418,406 to Ogawa (Ogawa) shows the signal wave control circuit which has the 2nd input side to the comparator for receiving an input signal, and the comparator for receiving a reference level signal. An output terminal conveys the output signal which has positive [corresponding to an input signal], and a negative portion. A detector detects the greatest or minimum transition interval included in an output signal in order to generate a detected signal. A hold circuit holds a detected signal, and when a control circuit generates a reference level signal, it is made for the interval of the positive portion of an output signal and the interval of the negative portion of an output signal to become equal. Therefore, said circuit is a system which eliminates the shift of DC-baseline, and an operation of an analog signal. This circuit needs the limited code system with which the run length which increases the record overhead of the data recorded as mentioned above was balanced. Therefore, a baseline regulation system with much more pliability more than what is shown in said Ogawa's patent is desired.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]The purpose of this invention is to provide DC baseline compensation which improved.
[0011]Another purpose of this invention is to provide the transition detection which detects transition, without paying the compensation of conquering the baseline shift in an input signal waveform, and increasing a noise.

MEANS

[Means for Solving the Problem]A baseline tracking threshold level detector by this invention pursues a motion of a baseline of an input data signal. A baseline shift is generated by being extracted from a rereading signal, i.e., an input signal, and sampling an input signal which tracking threshold level should detect, and adjusting detection threshold level as a baseline shift in data detection time.
[0013]In one aspect of affairs of this invention, a baseline position at the time of one detection, i.e., a sampling, holds a value of DC baseline detection threshold level till the next sampling. As for a sampling of an input data signal, it is preferred to attain by detecting a peak of an input analog signal, i.e., the point of inflection of transition.
[0014]In an example with this invention, a positive and negative peak detector specifies a peak envelope of a rereading signal, i.e., an analog signal, which should be detected. A peak value is equalized in order to find out detection threshold level. Subsequently, a tracking baseline is used as a standard which detects transition in specified sampling time.
[0015]In another example of this invention, a base line value is equalized among a series of transition position fields using the above-mentioned peak value equalization. In a specific form of this invention, a signal which should be detected is overdue by between [1 time of] patent periods. DC baseline tracking occurs between delay between 1 time of this patent period. In the end of the delay, amplitude of data in a signal to which tracking threshold level to an overdue signal was received and which was in it is detected correctly.
[0016]The above-mentioned of this invention and the other purposes, the feature, and an advantage become clear from the following explanation about a preferred embodiment of this invention shown in an accompanying drawing.

EXAMPLE

[Example]Refer to the accompanying drawing which directs the same member that has a structural feature for the same number below in the figure of ****. The portion 10 of an optical disc shows the track which has the track center line 15 which was recorded and was provided with the photodetection nature spots 11, 12, 13, and 14. The spot 11-14 can be detected in magneto-optics on a magneto-optics medium, or can perform detection of intensity modulation, for example like ablation medium (ablative) and phase change medium. The recorded spot 11-14 is in the flat face of said portion 10. That is, in this specific example, although the slot is not shown, it is understood that an optical medium with flatness or a slot can be adopted. This principle can be used also to the magnetic recording of a certain kind of type. In order to record the spot 11-14 showing the transition data 17, the record signal 16 is used. In this transition data 17, the binary 1 shows the transition in a transition position, and, on the other hand, binary zero show not being placed between the transition positions along the track 15 by transition. The information recorded on the mark 11-14 is drawn from the pulse temporal duration in the record

signal 16, i.e., the space between a series of transition, and provides the signal by which Pulse Density Modulation was carried out. Being able to apply the principle of this invention to pulse phase modulation, each of the positive peak position provided with the data 17 directs the only information as everyone knows to pulse position modulation. The reading signal 18 is acquired by detecting the information recorded on said portion 10. 1/2 wave with two long continuation shown for [11 and 12] the recorded wave-like imbalance (i.e., spots) shifts the DC baseline 19 of a rereading signal. According to this invention, the shift of the DC baseline 19 is adjusted in each of the transition position which the binary 1 in the data 17 shows.

[0018]Drawing 2 shows the conventional technology which the DC baseline 19 reads over also as a shift and carries out amplitude detection of the signal 18. He should understand that a possibility of a noise reading over, and it being introduced into a channel, and data losing, or acquiring error data is comparatively high. Generally, these systems are constituted to low density record, respectively. The noise produced by the rise of high frequency can introduce an error in a data detection process. Have often been called the jitter as shown in the parenthesis 33 which shows the variability region of the transition parts which were produced by the noise shown by the hash mark 34 of the signal 30, and which are not meant by this shift. According to one aspect of affairs of conventional technology, reading signal R reproduces the differential signal 25 which differentiates and has the fixed (dR/dt) baseline 26. The differentiated signal 25 acquires the signal 30 (dR'/dt) which differentiates again and has the baseline 31. Using 0 axis intersection of the signal 30, detection of the peak of the signal 25 is carried out at the time of **, and the data out signal 32 by which shaping detection was carried out is generated. It is necessary to remove the zero crossing which the signal 30 mistook by detecting the low amplitude portion of the signal 25, for example.

[0019]Drawing 3 shows 1 set of signal wave forms in which the principle which derives detection tracking amplitude threshold level, for example from an amplitude sample like the peak amplitude of the rereading signal 18 is shown. A detection process generates the positive signal envelope 40 and the negative signal envelope 41, and each envelope actually relates to the peak amplitude value positive [of the rereading signal 18 / each], and negative. The detection threshold level 42 pursues DC unbalanced shift of the baseline 19 by equalizing the value of the envelope signals 40 and 41 shifted with DC baseline. The reading signal 18 differentiates and the differential signal 25 is generated. Zero axes of the reading signal 18, i.e., baseline intersection, are in agreement with the signal 25 which differentiated peak amplitude in time. If there is peak amplitude of the differential signal 25 which is a peak of lower ******, the output pulses 43 and 44 will generate a peak and the threshold level 46 positive [exceeding the threshold level 45]. These pulses carry out the gate of 83 for the current source 67 into the temporal duration of positive [of the differential signal 25], and a negative pulse in order to make the storage capacitors 69 and 84 discharge. These capacitors memorize positive [which were received from the detectors 65 and 80, respectively], and a negative signal peak value, respectively. Discharge of each capacitor is generated just before detecting the following peak. By this discharge, tracking of a lower peak value is made possible (the amplitude of the signal peak of small amplitude is shown faithfully). When that is not right, the storage capacitors 69 and 84 can continue memorizing the peak value of high amplitude rather than preceding. The detected NRZI signal 32 is generated by detecting the signal 18 which crosses the baseline 42.

[0020]The value 42 of DC baseline, i.e., a detection tracking baseline, is held between 0 axis intersections of the reading signal 18. In zero axis each intersection of the reading signal 18, a baseline is measured again and detection threshold level is adjusted. Therefore, since this

amplitude drawn from the DC baseline 42 is thoroughly adjusted in each of 0 axis intersection of the reading signal 18, it pursues the shift of the baseline of the reading signal 18 promptly. This adjustment is generated twice to each of one perfect cycle of the reading signal 18. For example, in drawing 3, the 1st baseline adjustment draws a curve by the comparison 42A of the peak amplitude of the reading signals 40A and 41A. The 2nd adjustment in 42B shows the shift from the detection threshold level tracking level 42 of drawing 3 to the **** upper part. This adjustment is performed by measuring the amplitude difference between the peaks 40B and 41B. Small adjustment of 42A-1 which is adjustment is attained by the right peak detector 65 which acquires the positive peak 40B. This alignment procedure is repeated during signal processing of the rereading signal 18. The negative peaks 41A, 41B, and 41C are carried out in this way, and are pursued by the negative peak detector 80.

[0021]In this invention, 0 axis intersection of the reading signal 18 and the detection threshold level which pursues the baseline 42 equalize the amplitude of the peaks 40A and 41A. Therefore, it can be made to generate.

The equalizing circuit comprises the positive envelope buffer 68, the resistance 72, the negative envelope buffer 81, the resistance 85, and the equalization capacitor 73.

[0022]The transition which follows baseline measurement immediately is used in the 1st example. In the 2nd example, the transition located in the middle to the peak amplitude of the contiguity used in order to generate the corrected baseline detection threshold level is used. As for detection of data, and adjustment of a baseline, the detection threshold level 42, i.e., the baseline made to adjust, follows a shift and amplitude value of a rereading signal promptly very dynamically therefore. The signal wave form of the lot which can be used in order that drawing 4 may explain drawing 6 is shown, and tracking threshold level follows the baseline to shift based on the sampling of transition. This system is dynamic just like the thing explaining drawing 3, and is a preferred embodiment of present this invention. In this system, the rereading signal 18 is analyzed, makes the tracking threshold level 50 generate, and shifts this threshold level 50 with the shift of a baseline. The amplitude threshold level 52 and 53 of a lot detects the peak of the differential signal 25, and identifies 0 axis intersection of the reading signal 18. These values are adjusted in zero axis each intersection of the rereading signal 18. The reference numbers 54 and 55 show the sample of downward transition and the sample of rise transition in the signal 18, respectively, and they are sampled and equalized and derive detection threshold level.

[0023]After sampling and equalizing each denture (denture), it is made to memorize by the sample hold circuit mentioned later. This sample hold circuit holds the level of the drawn tracking threshold level 50. The signals 57 are positive [of the differentiated signal 25], and a group of the unipolar signal corresponding to the sampling aperture of negative transition. The NRZI rereading data signal 32 is generated by detecting the signal 18 which crosses the threshold level 50. Drawing 6 and drawing 7 show the detector circuit using the data detection art shown in drawing 4 which performs dynamic baseline shift adjustment.

[0024]Next, if drawing 5 is referred to, the optical disc 60 whose portion of 10 is a part of 3 will be detected in the usual way by the lens 61 and the optical apparatus 62 which can exercise using laser (not shown) so that focusing is possible. Relative focusing and positioning of the optical lens 61 to the optical disc 60 are common knowledge, therefore it is not explaining. Either of the optical apparatuses used for magneto-optics signal detection, phase change signal detection, etc. may be sufficient as the optical apparatus 62. To all the recording systems, the suitable reading signal detector 63 detects the recorded data, and supplies the signal 18 to the read amplifier 64, and this amplifier 64 supplies the amplified signal to the illustrated detector circuit.

[0025]The positive envelope signal 40 is generated by the circuit containing the right peak detector 65. This detector 65 supplies that positive peak detection signal to the operational amplifier 68. The capacitor 69 holds the peak value detected until the next transition was detected. If the next transition is detected, the differentiator 66 will generate the signal 25 from the rereading signal 18, and will be supplied to the GETEDO current source 67. If the signal 25 exceeds the positive threshold level 45, the GETEDO current source 67 will answer the positive peak of the differential signal 25, and will discharge the capacitor 69 promptly. If the storage capacitor 69 is discharged selectively, the right peak detector 65 will be charged at urgency to a new peak value as shows the capacitor 69 by 40B of drawing 3. Subsequently, the detected aforementioned value is held until it generates, as positive 0 axis intersection of the following shows by 40C of drawing 3. The operational amplifier 68 supplies the sample hold value memorized by the capacitor 69 to the resistance equalizing circuit containing the resistance 72 and 85 and the smoothing capacitor 73. The value held by the smoothing capacitor 73 is average value showing the detection tracking signal 42.
[0026]The negative peak envelope 41 is generated including the negative peak detector 80 by the circuit which supplies the value to the operational amplifier 81 and the storage capacitor 84. The same with having mentioned above about the positive peak, the capacitor 84 holds the value of the negative peak to the input side of the operational amplifier 81 until transition negative [next to the reading signal 18] is detected. That is, this signal is held until it comes to have the negative peak amplitude in which the signal 25 is lower than the amplitude threshold level 46. The differentiator 82 differentiates the signal 18 again and supplies the differentiated signal to the GETEDO current source 83. The GETEDO current source 83 answers the lower **** signal 25 in the negative threshold level 46, and discharges the capacitor 84 promptly. After the storage capacitor 84 is discharged selectively, in the negative peak value which charged the capacitor 84 promptly and from which the reading signal 18 was detected exactly, the negative peak detector 80 resets up the negative envelope value 41. The operational amplifier 81 supplies the signal 41 to the capacitor 73 via the resistance 85. It has impedance with the equal resistance 72 and 85, therefore the mean value between two peaks, positive [which was detected continuously] and negative, is found out, and the signal 42 is generated.
[0027]Data detection is attained by three elements shown in drawing 5. In order that a comparison circuit may compare with the signal 42, the signal 18 is received via the line 75. The NRZI signal from this comparison is supplied to analog circuitry AND86, and analog circuitry AND86 is energized and generates a series of pulses which show the NRZI data output shown as the signal 32 in drawing 3 on the line 88. Only when the data signal is detected, AND86 enables it for the gap gate 87 to let the digital signal 32 pass from the comparator 74 to the line 88. Positive [of exceeding or the lower **** signal 25] and a negative peak generate the pulses 43 and 44 for the positive and negative thresholds 45 and 46, respectively. Since the gap gating function 87 is produced, the pulses 43 and 44 are used. The gap gate 87 answers the signal 25 supplied by the differentiator 82, and directs when an authentic data signal is received. In many records, it is between the blocks with which the signal was recorded, a gap, i.e., a field, without a signal. The gap gate 87 detects the block of such a gap or a signal in a well-known way, for example according to envelope detection, integration, etc. The gap gate 87 carries out the gate of the signal 32 detected from the comparator via the AND date 86.
[0028]Drawing 6 shows the circuit which performs the transition position detection phase of this invention. The operational amplifier 64 supplies the amplified rereading signal 18 to the comparison circuit 90 via the line 91. The rereading signal 18 is supplied to sample hold circuit

S&H 92, and as this circuit 92 was started and drawing 4 was explained, it samples a signal again. The differentiator 94 generates the signal 25, and this signal exceeded the threshold level 52, or makes the sample gate 95 it to be compared with the amplitude threshold level 52 and 53, and energize the threshold level 53 to an amplitude working range positive [of the lower ****** signal 25], and negative about this point. A series of two integration with the sample hold amplitude 54 and 55 is supplied to the integrating capacitor 93, and supplies the signal 50 to the comparison circuit 90. The integration of the signal in the capacitor 93 is the integration of time and amplitude, and gives directions of transition. As for the capacitor 93, it is large enough to it being few and making it make that the detection threshold level 50 shifts more nearly dynamically than the threshold level 42. The NRZI pulse 32 occurs by the result of the comparison 90 between the reading signal 18 and the threshold level 50.

[0029]Drawing 7 shows the circuit which detects 0 axis intersection of the signal 18. The line 75 carries the signal of the operational amplifier 64 to the differentiator 100, and this differentiator 100 generates the signal 25 (drawing 4). The signal 25 follows even the peak amplitude comparison detection machines 101 and 102 of a couple. The comparator 101 has the reference value supplied by the potentiometer 103, and generates the voltage threshold level 52. The comparator 101 supplies the fixed amplitude signal which is sampled in the circuit 110, is held and is equalized to OR gate 105. Similarly, to the negative working range of the differentiated signal 25, the potentiometer 104 supplies the voltage threshold level 53, and this threshold level 53 is supplied to the reference input side of the switching comparator 102. the signal 25 -- the threshold level 53 -- lower ****** -- a gating signal is supplied to OR circuit 105, and it lets when pass to a sample, equalization, and the hold circuit 110. Gating pulses are the same temporal duration and the same amplitude.

Therefore, these signals should note reading over in contrast with the peak amplitude used to the example shown in drawing 5, and expressing a transition position.

[0030]Drawing 8 shows the suitable structure of the sample, equalization, and hold circuit which is publicly known composition. The signal of the line 113 is supplied as an input to the switching amplifier 120. The peak indication signal on the line 106 supplied by OR circuit 105 makes the charge pump 120 one, samples the amplitude of the signal 18, and compares it with the current value of the detection threshold level signal 50 on the line 112. The amplitude difference detected by the circuit 120 between an input value and a reference current value adjusts the voltage memorized by the capacitor 121 into the temporal duration of the peak instruction pulse 57. The memorized value continues being supplied to the operational amplifier 122, and this amplifier 122 supplies the tracking detection threshold level signal 50 on the line 112. The sample, equalization and hold-circuit S&H 92 of drawing 6, and the capacitor 93 are substituted for the circuit shown in drawing 8.

[0031]Although this invention has been illustrated and explained especially with reference to a preferred embodiment, in a gestalt and details, what can be changed is understood variously, without deviating from the pneuma and the range of this invention to the specialist in the technical field concerned.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1]They are some schematic diagrams of the optical disc which records on it the signal

by which Pulse Density Modulation was carried out, and has a rereading signal of the result.
[Drawing 2]It is a figure showing the detection system of conventional technology using the differentiated signal.
[Drawing 3]It is a graph which shows two or more signals used in order to show operation of this invention.
[Drawing 4]It is a figure showing the amended detecting method by this invention.
[Drawing 5]It is a diagram showing one detector circuit which performed this invention.
[Drawing 6]It is a diagram showing another detector circuit which performed this invention.
[Drawing 7]Furthermore it performed this invention, it is a diagram showing another detector circuit.
[Drawing 8]It is a diagram showing the sample, equalization, and hold circuit which can be used with the detector circuit shown in drawing 7.
[Description of Notations]
60: An optical disc and 65 : a positive peak detector,
66, 82, a 94,100:differentiator, 67, 83: **-**** current source
68, an 81,122:operational amplifier, 74, 90: Comparison circuit
87, 96:gap gate, and 86: Analog circuitry AND
92: A sample hold circuit and 95 : sample gate
101,102: A comparison-detection machine and 105: OR gate
110: A sample, equalization and a hold circuit, and 120 : switching amplifier

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[Translation done.]

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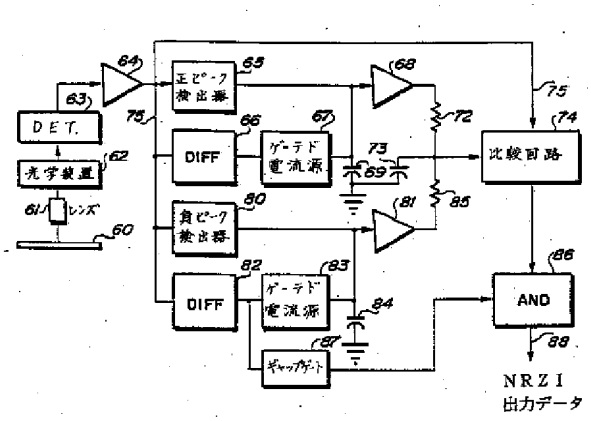
最終頁に続く

(54)【発明の名称】　デジタルデータ信号を検出する装置および方法

(57)【要約】　（修正有）

【目的】　入力信号波形のベースラインシフトを克服しかつノイズの増大なしの遷移検出をする。

【構成】　検出されつつある信号のベースラインにおける後続のシフトに対して検出スレッショルドを調整するために振幅又は遷移位置のいずれかの技術を採用しているデータ検出回路が設けられる。振幅技術の場合、検出された一連の正と負のピーク間の中間振幅値が、平均化コンデンサ73に保持され、スレッショルド調整が一回の検出期間において行われ、かつすぐ後続の検出期間において用いられるように、検出スレッショルドを調整する。追跡検出スレッショルドによりアナログ信号の零軸交差を検出してＮＲＺＩデジタル波形をアナログＡＮＤ回路81で発生させる。また、遷移位置検出の場合は、読取り信号の遷移のサンプリングによって表わされる一連の遷移の時間的な相対位置が積分され、平均化されてベースラインシフトを追跡する検出を行う。



【特許請求の範囲】
【請求項１】　検出すべきデジタル情報を運ぶデータ信号を受け取る手段と、
受け取られたデータ信号を微分して、該微分された信号を供給する手段と、
前記微分された信号を受け取り、その正と負のピークを検出して、各々の検出されたピークに対して、受け取られたデータ信号中の遷移と一致するサンプリングアパーチャを提供するピーク回路手段と、
前記受け取る手段に接続されて前記受け取られたデータ信号を受け取り、かつ前記ピーク回路手段に接続されて各サンプリングアパーチャ信号に応答して、遅れて受け取られたデータ信号のそのときの電流値を、ベースラインを指示する値としてサンプリングし記憶するサンプル・ホールド回路手段と、
前記サンプル・ホールド回路手段に接続され、受け取られたデータ信号の、次に発生する遷移を示す零軸交差のための値を示す前記ベースラインを使用して、受け取られたデータ信号により指示されたデータの値を検出する検出回路手段と、
を含む、デジタルデータ信号を検出する装置。
【請求項２】　前記サンプル・ホールド回路手段が一連の異なる極性の遷移サンプルの値を平均化する平均化手段を含む請求項１に記載のデジタルデータ信号を検出する装置。
【請求項３】　前記データ信号のＤＣベースラインのレベルルシフトを検出し、前記ベースラインと共にシフトする検出スレッショルドをセットし、
前記データ信号における次に連続するデータ遷移に対して前記検出スレッショルドを用いてデータ信号を振幅検出するステップを含むデータ信号を検出する方法。
【請求項４】　前記データ信号のピーク振幅の１つを測定し、次に前記の１つのピーク振幅と反対の信号極性を有する前記データ信号の次の１つのピーク振幅を測定し、
前記の測定されたピーク振幅の２つの値を平均化することにより前記検出スレッショルドを生成するステップをさらに含む請求項３に記載の方法。
【請求項５】　前記データ信号を微分し、
該微分された信号ピーク振幅が、所定の正の振幅スレッショルドを上廻る又は所定の負の振幅スレッショルドを下廻るときのみ、該微分された信号のピークを検出することにより前記ベースラインレベルシフトを検出するステップをさらに含む請求項４に記載の方法。
【請求項６】　データが検出可能である検出期間を有するデータ信号において遷移を検出する装置において、
信号の各々の検出期間においてデータ信号の単一のエンベロップを分析し、次に発生する検出期間に対して前記の分析された信号エンベロップに対する所定の振幅関係を有する振幅検出スレッショルドを設定する第１の手段と、
データ信号の次に発生する検出期間において前記データ信号と前記振幅検出スレッショルドとを振幅比較する第２の手段とを含む、データ信号の遷移を検出する装置。
【請求項７】　前記データ信号が各検出期間において複数のピーク振幅を有しており、
前記第１の手段は、２つの反対のピークの振幅を検出するピーク検出手段と、前記ピーク検出手段に接続され検出されたピーク振幅を平均化し、前記の平均を前記振幅検出スレッショルドとして供給する平均化手段とをさらに含む請求項６に記載の装置。
【請求項８】　前記第１の手段は、前記データ信号を微分する微分手段を有し、
前記ピーク検出手段は、前記微分手段に結合され、前記の微分されたデータ信号の２つのピークの振幅をピーク検出する請求項７に記載の装置。
【請求項９】　前記の検出されたデータ信号を受け取るために前記第２の手段に接続されたゲート手段と、
真正のデータ信号が受け取られているときを指示するために前記データ信号を受け取り、かつ前記ゲート手段を付勢して前記真正の信号が指示されたときのみ検出されたデータ信号を通すギャップ手段とをさらに含む請求項６に記載の装置。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明はデータ検出器に関し、特にパルス幅変調（ＰＷＭ）と共に使用可能で、光ディスクレコーダと共に使用する検出器に関する。
【０００２】
【従来の技術】デジタルあるいは二極信号が、一方あるいは他方の極性に向かって不均衡となるときは常にデジタルあるいはデジタル化した信号処理は信号のベースラインシフトに対して影響されやすく、優勢の極性に向かうシフトはベースラインをその極性に向けて移動させる。
【０００３】図１に示すＮＲＺＩパターン１６のようなデジタル波形（バイナリ信号としても知られている）は何らベースラインシフトしておらず、これはその波形にはレベルが２つあるのみであることを意味する。波形はＨＩで種辞する高レベルと、ＬＯで指示する低レベルと、Ｔで指示する２レベルの間の遷移部分とを有する。デジタル波形の理想的な再生は、ノイズの無い、バンド帯が無限の直線アナログチャンネルを要する。
【０００４】磁気テープ書込み／読取りチャンネルあるいは光ディスク書込み／読取りチャンネルのようなアナログチャンネルをデジタル波形が通るときは歪を経験する。歪は、主としてチャンネルのバンド帯が制限されていることと、ノイズが加わることによって生ずる。チャンネルの高周波数限度即ち高周波数ロールオフにより、高周波数（即ち波長の短い）信号は低周波数（即ち波長

の長い）信号より振幅が小さくなる。波形即ち信号１８は高周波数のロールオフ歪を示す。信号処理回路の種々のステージ間のＤＣシフト並びにドリフトを排除するためにチャンネルにおいて採用したＡＣカップリングにより、信号のＤＣ成分、従ってベースラインシフトを除去する。ベースラインとは、アナログ波形の隣接する２つの反対側のピーク間の平均点を結ぶ理想線である。ベースラインシフトを参照番号１９で示す。波長とデジタルシーケンスとに応じて、高周波数ロールオフとＡＣカップリグの双方により、アナログ信号はそのベースラインをシフトする。光デイスクチャンネルにおける読返し信号のベースラインが動く別の原因は光デイスク基板の媒体反射率と複屈折の変化である。前述の理由により、アナログ波形のピークと遷移とは、種々の、度々予測できないレベルにおいて発生し、従来のスレッショルド固定の検出器では信頼性よく検出するのが困難である。

【０００５】データ検出器においては、ベースラインシフトは、遷移位置を見掛け上シフト（ベースラインシフトに伴なう零軸交差のシフト）させる可能性がある。ベースラインシフトを若干でも許容あるいは阻止する一方法は、均衡したコードを提供することである。即ち、一方の極性の信号の量が他方の極性の信号の同じ量と等しく、そのため信号の正味のＤＣ成分が零となるようにすることである。このため、記録されたデータのオーバヘッドを増し、従って、信号ベースラインにおけるいずれかのＤＣシフトも迅速に補償するデータ検出システムを提供することが望ましい。

【０００６】デジタル情報を運ぶアナログデータ遷移を検出する最も単純な方法は、例えば、アナログデータ波形の振幅を一定の振幅のスレッショルドと比較することである。そのような検出においては、アナログ信号の振幅がスレッショルドを交差する毎に遷移が示される。アナログ遷移の傾斜、即ち零軸交差部の傾斜は、読取チャンネルバンド幅とその特性を含む多くのファクタによって変わる。一般的に、バンド幅が小さければ小さいほど、傾斜は小さい。傾斜が小さければ小さいほど、パルス幅変調された信号を検出する上で必要な零軸交差の正確な位置を得ることが難しい。また、アナログ信号ベースライン（ＤＣレベル）は常に動いていることは周知である。遷移部と一定のスレッショルドとの間の実際の交差点がシフトしデータ検出エラーを発生させる。もしアナログ信号が固定のスレッショルドの完全に上方、あるいは下方を動くとすれば、遷移の検出はうまくできない。アナログ信号に戻される読返し信号の光デイスクのベースライン移動により、度々使用される交流（ＡＣ）カップリングのためいずれかの極性に向かってシフトし、かつ動的に変動し、媒体の反射率と、読取り、即ち検出レーザビームがそこを通って光媒体の記録層に達する基板の複屈折とによって変動する。

【０００７】前述のベースラインシフトのために、一般的な遷移検出方法は、受け取られたアナログ信号を微分し、次に微分した信号をピーク検出する方法である。微分した信号は、零軸交差を得るために再微分されることが多く、零軸交差は微分した信号の各ピークと時間的に一致している。これらの零軸交差を検出することにより二つの零軸交差が検出される。微分検出に係わる問題は、微分過程に付随するノイズの増加である。勿論微分により、読取りチャンネルにおける高周波数応答性を増大させ、高周波数ノイズを上昇させる。理論的には、信号対ノイズ比の低減は約６デジベルである。前記の問題を排除し、この検出法をベースラインシフトに適用してベースラインに対する感度を低減させることが望ましい。

【０００８】読取り信号の微分はまた、検出を調時するためにも使用される。即ち、微分した信号の零交差は読取り信号のピークと時間的に一致する。マーチャント他（Ｍａｒｃｈａｎｔ　ｅｔ　ａｌ）への米国特許第４，４７５，１８３号はそのようなシステムを示している。このシステムも、排除すべきである、検出過程での遷移位置の位相シフトに影響される。

【０００９】オガワ（Ｏｇａｗａ）への米国特許第４，４１８，４０６号は、入力信号を受け取るための比較器と、基準レベル信号を受け取るための比較器への第２の入力側を有する信号波制御回路を示している。出力端子は、入力信号に対応する正と負の部分とを有する出力信号を搬送する。検出器は、検出済信号を発生させるために出力信号に含まれる最大あるいは最小の遷移間隔を検出する。ホールド回路は検出済信号をホールドし、制御回路は基準レベル信号を発生させることによって出力信号の正の部分の間隔と出力信号の負の部分の間隔とが等しくなるようにする。従って、前記回路は、ＤＣ－ベースラインのシフトとアナログ信号の作用を排除するシステムである。この回路は、前述のように記録されたデータの記録オーバヘッドを増大させる走行長さの均衡した限定コードシステムを必要とする。従って、前記オガワの特許に示されているもの以上の一層の柔軟性のあるベースライン調節システムが望まれる。

【００１０】

【発明が解決しようとする課題】本発明の目的は、向上したＤＣベースライン補償を提供することである。

【００１１】本発明の別の目的は、入力信号波形におけるベースラインシフトを克服し、かつ、ノイズを増大するという代償を払うことなく遷移を検出する遷移検出を提供することである。

【００１２】

【課題を解決するための手段】本発明によるベースライントラッキングスレッショルド検出器は入力データ信号のベースラインの動きを追跡する。ベースラインシフトは、読返し信号即ち入力信号から抽出され、トラッキングスレッショルドが、検出すべき入力信号をサンプリン

グし、かつ、データ検出時間におけるベースラインシフトとして検出スレッショルドを調整することにより生成される。

【００１３】本発明の一局面においては、一回の検出時即ちサンプリング時のベースライン位置は、次のサンプリング時までＤＣベースライン検出スレッショルドの値を保持する。入力データ信号のサンプリングは、入力アナログ信号のピーク即ち遷移の変曲点を検出することにより達成することが好ましい。

【００１４】本発明のある実施例においては、正と負のピーク検出器は、検出すべき読返し信号即ちアナログ信号のピークエンベロップを規定する。検出スレッショルドを見い出すためにピーク値は平均化される。次いでトラッキングベースラインは、規定されたサンプリング時間において遷移を検出する基準として使用される。

【００１５】本発明の別の実施例において、ベースライン値は、前述のピーク値平均化を用いて一連の遷移位置領域の間で平均化される。本発明の特定形態においては、検出すべき信号は、１回の検出期間分遅れる。この１回の検出期間の遅れの間、ＤＣベースライントラッキングが発生する。その遅れの終りにおいて、遅れた信号に対するトラッキングスレッショルドが、受け取られかつ遅れた信号におけるデータの振幅を正確に検出する。

【００１６】本発明の前述およびその他の目的、特徴および利点は、添付図面に示す本発明の好適実施例についての以下の説明から明らかとなる。

【００１７】

【実施例】数葉の図において、同じ番号が構造上の特徴を有する同じ部材を指示する添付図面を以下参照する。光デイスクの部分１０は、記録されかつ光検出性スポット１１、１２、１３および１４を備えたトラック中心線１５を有するトラックを示す。スポット１１－１４は、磁気光学的媒体上で磁気光学的に検出できるか、あるいは、例えば、アブレーションな（ａｂｌａｔｉｖｅ）媒体や位相変更媒体のように、強度変調の検知ができる。記録されたスポット１１－１４は、前記部分１０の平坦面にある。即ち、この特定の実施例においては、溝は示されていないが、平坦あるいは溝付きの光学媒体を採用しうることが理解される。さらに、この原理は、ある種のタイプの磁気記録に対しても使用しうる。遷移データ１７を表わすスポット１１－１４を記録するために、記録信号１６が使用される。この遷移データ１７においては、バイナリ１は遷移位置における遷移を示し、一方バイナリゼロは、トラック１５に沿った遷移位置に遷移が介在しないことを示す。マーク１１－１４に記録された情報は、記録信号１６におけるパルスお持続時間から、即ち一連の遷移の間のスペースから導出され、パルス幅変調された信号を提供する。本発明の原理はまた、パルス位相変調に適用でき、データ１７により提供される正のピーク位置の各々は、パルス位置変調に対して周知のように唯一の情報を指示する。前記部分１０に記録された情報を検出することにより読取り信号１８が得られる。記録された波形の不均衡のため、即ちスポット１１と１２で示す２つの連続の長い２分の１波長は、読返し信号のＤＣベースライン１９をシフトする。本発明によれば、ＤＣベースライン１９のシフトは、データ１７におけるバイナリ１が示す遷移位置の各々において調整される。

【００１８】図2は、ＤＣベースライン１９がシフトとしても読返し信号１８を振幅検出する従来技術を示す。ノイズが読返しチャンネルに導入され、データが喪失したり、あるいはエラーデータを取得する可能性は比較的高いことを理解すべきである。一般的に、これらのシステムは、それぞれ低密度記録に対して構成されている。高周波数の上昇により生じるノイズが、データ検出過程においてエラーを導入しうる。このシフトは、信号３０のハッシュマーク３４により示すノイズにより生じた意図しない遷移部分の変化範囲を示す括弧３３で示すようなジッタと称されることがよくある。従来技術の一局面によれば、読取り信号Ｒは微分されて（ｄＲ／ｄｔ）一定のベースライン２６を有する微分信号２５を再生する。微分された信号２５は、再度微分されてベースライン３１を有する信号３０（ｄＲ′／ｄｔ）を得る。信号３０の零軸交差を用いて、信号２５のピークの検出を調時し、成形検出されたデータ出力信号３２を発生する。信号３０の誤った零交差は、例えば信号２５の低振幅部分を検出することにより除去する必要がある。

【００１９】図3は、例えば読返し信号１８のピーク振幅のような振幅サンプルから検出トラッキング振幅スレッショルドを導出する原理を示す１組の信号波形を示す。実際、検出過程は、正の信号エンベロップ４０と負の信号エンベロップ４１とを発生させ、各エンベロップは読返し信号１８の各々の正と負のピーク振幅値に関連している。検出スレッショルド４２は、ＤＣベースラインと共にシフトするエンベロップ信号４０、４１の値を平均化することによりベースライン１９のＤＣ非均衡シフトを追跡する。さらに、読取り信号１８が微分されて微分信号２５を発生させる。読取り信号１８の零軸即ちベースライン交差は、ピーク振幅を微分した信号２５と時間的に一致する。スレッショルド４５を越える正のピークとスレッショルド４６を下廻る負のピークである微分信号２５のピーク振幅があると出力パルス４３、４４が発生する。これらのパルスは、記憶コンデンサ６９、８４を放電させるために微分信号２５の正と負のパルスの持続時間中に電流源６７を８３とをゲートする。これらのコンデンサは、それぞれ検出器６５、８０から受け取られた正と負の信号ピーク値をそれぞれ記憶する。各コンデンサの放電は次のピークを検出する直前に発生する。この放電により、より低いピーク値のトラッキングを可能とする（より忠実に小さい振幅の信号ピークの振

幅を示す）。そうでない場合は、記憶コンデンサ６９、８４は先行するより高い振幅のピーク値を記憶し続けることができる。検出されたＮＲＺＩ信号３２は、ベースライン４２を交差する信号１８を検出することにより発生する。

【００２０】ＤＣベースラインの値即ち検出トラッキングベースライン４２が、読取り信号１８の零軸交差の間で保持される。読取り信号１８の各零軸交差において、ベースラインが再度測定され、検出スレッショルドが調整される。従って、ＤＣベースライン４２から導出されたこの振幅は、読取り信号１８の零軸交差の各々において完全に調整されるため読取り信号１８のベースラインのシフトを迅速に追跡する。この調整は、読取り信号１８の完全な一サイクルの各々に対して、２回発生する。例えば図３において、第１のベースライン調整は、読取り信号４０Ａと４１Ａのピーク振幅の比較４２Ａで曲線を描く。４２Ｂにおける第２の調整では、図３の検出スレッショルドトラッキングレベル４２から視て上方へのシフトを示している。この調整は、ピーク４０Ｂと４１Ｂとの間の振幅差を測定することにより行われる。小さい調整である４２Ａ－１の調整は、正のピーク４０Ｂを取得する正ピーク検出器６５により達成される。この調整過程は、読返し信号１８の信号処理中に繰り返される。負のピーク４１Ａ、４１Ｂおよび４１Ｃは、このようにして負ピーク検出器８０により追跡される。

【００２１】本発明によれば、読取り信号１８の零軸交差と、ベースライン４２を追跡する検出スレッショルドとは、ピーク４０Ａと４１Ａの振幅を平均化することにより生成させることができる。平均化回路は正のエンベロップバッファ６８、抵抗７２、負のエンベロップバッファ８１、抵抗８５および平均化コンデンサ７３から構成されている。

【００２２】第１の実施例においては、ベースライン測定にすぐ続く遷移が使用される。第２の実施例においては、訂正されたベースライン検出スレッショルドを発生させるために使用される隣接のピーク振幅に対して中間に位置する遷移が使用される。データの検出とベースラインの調整とは、極めて動的であって、そのため検出スレッショルド４２即ち調整させたベースラインが、読返し信号のシフトと振幅値とに迅速に追従する。図４は、図６を説明するために使用しうる一組の信号波形を示し、トラッキングスレッショルドは、遷移のサンプリングに基いて、シフトするベースラインに追従する。このシステムは、図３について説明したものと正に同様に動的であり、かつ現在本発明の好適実施例である。このシステムにおいては、読返し信号１８は、分析されて、トラッキングスレッショルド５０を生成させ、このスレッショルド５０は、ベースラインのシフトと共にシフトする。一組の振幅スレッショルド５２と５３とが、微分信号２５のピークを検出し、読取り信号１８の零軸交差を識別する。これらの値は、読返し信号１８の各零軸交差において調整される。参照番号５４と５５とは、信号１８における下降遷移のサンプルと上昇遷移のサンプルとをそれぞれ示し、それらは、サンプリングされかつ平均化され、検出スレッショルドを導出する。

【００２３】各々のデンチャ（ｄｅｎｔｕｒｅ）をサンプリングし平均化した後、後述するサンプル・ホールド回路により記憶させる。このサンプル・ホールド回路は、導出されたトラッキングスレッショルド５０のレベルを保持する。信号５７は、微分した信号２５の正と負の遷移のサンプリングアパーチャに対応する単極信号の組である。ＮＲＺＩ読返しデータ信号３２は、スレッショルド５０を交差する信号１８を検出することにより発生する。図６と図７とは、動的なベースラインシフト調整を行う図４に示すデータ検出技術を用いる検出回路を示す。

【００２４】次に図５を参照すれば、１０の部分が３の一部である光デイスク６０がレーザ（図示せず）を用い、焦点合わせ可能で、かつ運動可能のレンズ６１と光学装置６２とにより通常の要領で検出される。光デイスク６０に対する光学レンズ６１の相対的な焦点合わせと位置決めとは周知であり、そのため説明していない。光学装置６２は、磁気光学信号検出、位相変化信号検出等に用いられる光学装置のいずれかでよい。全ての記録システムに対して適切な読取り信号検出器６３は、記録されたデータを検出し、信号１８を読取り増幅器６４に供給し、該増幅器６４は、増幅された信号を、図示した検出回路に供給する。

【００２５】正のエンベロップ信号４０は、正ピーク検出器６５を含む回路によって発生する。この検出器６５は、その正のピーク検出信号を演算増幅器６８に供給する。コンデンサ６９は、次の遷移が検出されるまで検出されたピーク値を保持する。次の遷移が検出されると、微分器６６は、読返し信号１８からの信号２５を発生させ、ゲーテド電流源６７に供給する。信号２５が正のスレッショルド４５を上廻ると、ゲーテド電流源６７は、微分信号２５の正のピークに応答してコンデンサ６９を迅速に放電する。記憶コンデンサ６９が部分的に放電されると、正ピーク検出器６５は、コンデンサ６９を例えば図３の４０Ｂで示すような新しいピーク値まで急速に充電する。次いで、前記の検出された値は、次の正の零軸交差が例えば図３の４０Ｃで示すように発生するまで保持される。演算増幅器６８は、コンデンサ６９に記憶されたサンプル・ホールド値を抵抗７２、８５および平滑化コンデンサ７３とを含む抵抗平均化回路に供給する。平滑化コンデンサ７３により保持された値は、検出トラッキング信号４２を表わす平均値である。

【００２６】負のピークエンベロップ４１は、負ピーク検出器８０を含み、その値を演算増幅器８１と記憶コンデンサ８４とに供給する回路により発生する。コンデン

サ８４は、正のピークについて前述したのと同様に演算増幅器８１の入力側への負のピークの値を、読取り信号１８の次の負の遷移が検出されるまで保持する。即ち、この信号は、信号２５が振幅スレッショルド４６より低い負のピーク振幅を有するようになるまで保持される。微分器８２は、再度信号１８を微分し、微分した信号をゲーテド電流源８３に供給する。ゲーテド電流源８３は、負のスレッショルド４６を下廻る信号２５に応答して迅速にコンデンサ８４を放電する。記憶コンデンサ８４が部分的に放電された後、負ピーク検出器８０は、コンデンサ８４を迅速に充電して読取り信号１８の丁度検出された負のピーク値において負のエンベロップ値４１を設定し直す。演算増幅器８１は、信号４１を抵抗８５を介してコンデンサ７３に供給する。抵抗７２と８５とは、等しいインピーダンスを有し、従って２つの連続して検出された正と負のピーク間の中間値を見い出して信号４２を発生させる。

【００２７】データ検出は、図５に示す３つの要素により達成される。比較回路が、信号４２と比較するために、ライン７５を介して信号１８を受け取る。この比較からのＮＲＺＩ信号は、アナログ回路ＡＮＤ８６に供給され、アナログ回路ＡＮＤ８６は、付勢されて、図３において信号３２として示されているＮＲＺＩデータ出力を示す一連のパルスをライン８８上に発生させる。ギャップゲート８７は、データ信号が検出されているときのみＡＮＤ８６がデジタル信号３２を比較器７４からライン８８まで通すことができるようにする。正と負のしきい値４５、４６をそれぞれ上廻り又は下廻る信号２５の正と負のピークが、パルス４３と４４とを発生させる。パルス４３と４４とは、ギャップゲーティング機能８７を生ずるために使用される。ギャップゲート８７は、微分器８２によって供給された信号２５に応答して、いつ真正データ信号が受け取られるかを指示する。多くの記録では、信号の記録されたブロック間に信号の無いギャップ即ち領域がある。ギャップゲート８７は、例えばエンベロップ検出、積分等により周知の要領でそのようなギャップや信号のブロックを検出する。ギャップゲート８７は、ＡＮＤデート８６を介して比較器からの検出された信号３２をゲートする。

【００２８】図６は、本発明の遷移位置検出局面を実行する回路を示す。演算増幅器６４は、増幅された読返し信号１８をライン９１を介して比較回路９０に供給する。読返し信号１８はまた、サンプル・ホールド回路Ｓ＆Ｈ　９２に供給され、該回路９２は起動されて図４に関して説明したように信号をサンプリングする。この点に関して、微分器９４は、信号２５を発生し、該信号は、振幅スレッショルド５２および５３と比較され、スレッショルド５２を上廻った又はスレッショルド５３を下廻った信号２５の正と負の振幅動作範囲に対してサンプルゲート９５を付勢させる。サンプル・ホールド振幅５４と５５との２つの一連の積分が、積分コンデンサ９３に供給され信号５０を比較回路９０に供給する。コンデンサ９３における信号の積分は、時間と振幅の積分であって遷移の指示を与える。コンデンサ９３は、検出スレッショルド５０がスレッショルド４２より動的にシフトすることが少ないようにさせるに十分大きい。読取り信号１８とスレッショルド５０との間の比較９０の結果によりＮＲＺＩパルス３２が発生する。

【００２９】図7は、信号１８の零軸交差を検出する回路を示す。ライン７５は、演算増幅器６４の信号を微分器１００まで運び、該微分器１００は、信号２５を発生する（図４）。信号２５は、一対のピーク振幅比較検出器１０１、１０２まで進む。比較器１０１は、ポテンショメータ１０３により供給された基準値を有し、電圧スレッショルド５２を発生する。比較器１０１は、回路１１０でサンプリングされホールドされ、平均化される一定の振幅信号をＯＲゲート１０５へ供給する。同様に、微分された信号２５の負の動作範囲に対して、ポテンショメータ１０４は、電圧スレッショルド５３を供給し、該スレッショルド５３は、スイッチング比較器１０２の基準入力側に供給される。信号２５がスレッショルド５３を下廻ればいつでも、ゲート信号が、ＯＲ回路１０５へ供給され、サンプル・平均化・ホールド回路１１０まで通される。ゲーティングパルスは、同じ持続時間、同じ振幅であり、従ってこれらの信号は、図５に示した実施例に対して用いられたピーク振幅とは対照的に読返し遷移位置を表わすことに注目すべきである。

【００３０】図8は、公知の構成であるサンプル・平均化・ホールド回路の好適構造を示す。ライン１１３の信号は、スイッチング増幅器１２０への入力として供給される。ＯＲ回路１０５によって供給された、ライン１０６上のピーク指示信号が、チャージポンプ１２０をオンにして信号１８の振幅をサンプリングし、それをライン１１２上の検出スレッショルド信号５０の現在の値と比較する。入力値と電流基準値との間の、回路１２０によって検出された振幅差は、ピーク指示パルス５７の持続時間中に、コンデンサ１２１に記憶された電圧を調整する。記憶された値は、演算増幅器１２２に供給され続け、該増幅器１２２は、ライン１１２上にトラッキング検出スレッショルド信号５０を供給する。図８に示す回路は、図６のサンプル・平均化・ホールド回路Ｓ＆Ｈ　９２とコンデンサ９３とに代替する。

【００３１】本発明を特に好適実施例を参照して図示し、かつ説明してきたが、当該技術分野の専門家には本発明の精神と範囲とから逸脱することなく形態および細部において種々変更が可能なることが理解される。

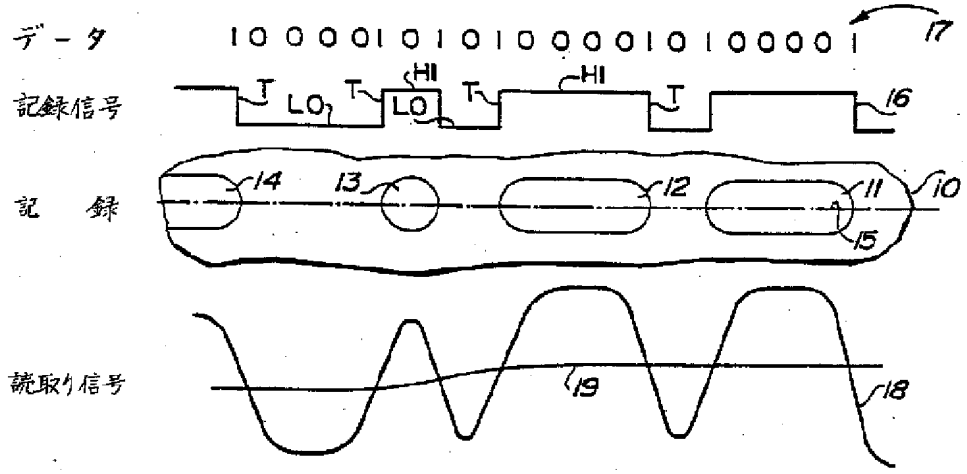
【図面の簡単な説明】

【図１】パルス幅変調された信号をその上に記録し、その結果の読返し信号を有する光デイスクの一部の概略図である。

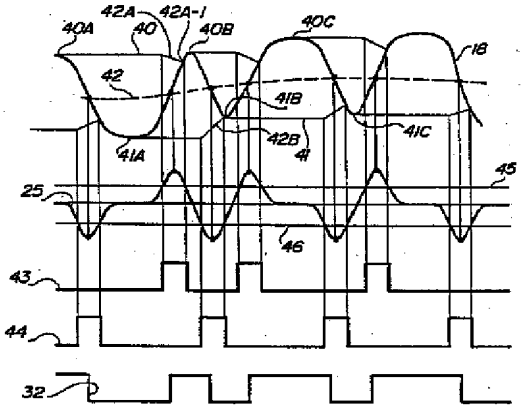
【図２】微分された信号を用いる従来技術の検出システムを示す図である。
【図３】本発明の動作を示すために用いた複数の信号を示すグラフである。
【図４】本発明による修正された検出方法を示す図である。
【図５】本発明を実行した１つの検出回路を示す線図である。
【図６】本発明を実行した別の検出回路を示す線図である。
【図７】本発明を実行した更に別の検出回路を示す線図である。
【図８】図７に示す検出回路と共に使用しうるサンプル・平均化・ホールド回路を示す線図である。

【符号の説明】
６０：光デイスク、　６５：正ピーク検出器、
６６，８２，９４，１００：微分器、　６７，８３：ゲーテド電流源
６８，８１，１２２：演算増幅器、　７４，９０：比較回路
８７，９６：ギャップゲート、　８６：アナログ回路ＡＮＤ
９２：サンプル・ホールド回路、　９５：サンプルゲート
１０１，１０２：比較検出器、　１０５：ＯＲゲート
１１０：サンプル・平均化・ホールド回路、　１２０：スイッチング増幅器

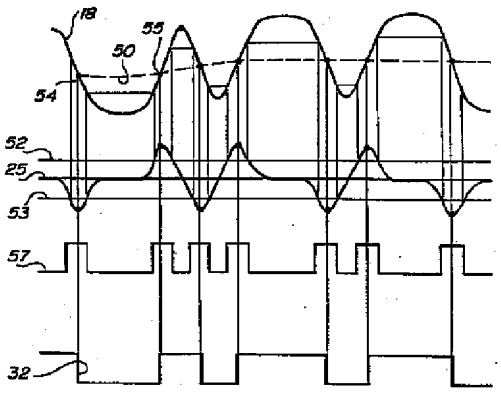
【図１】



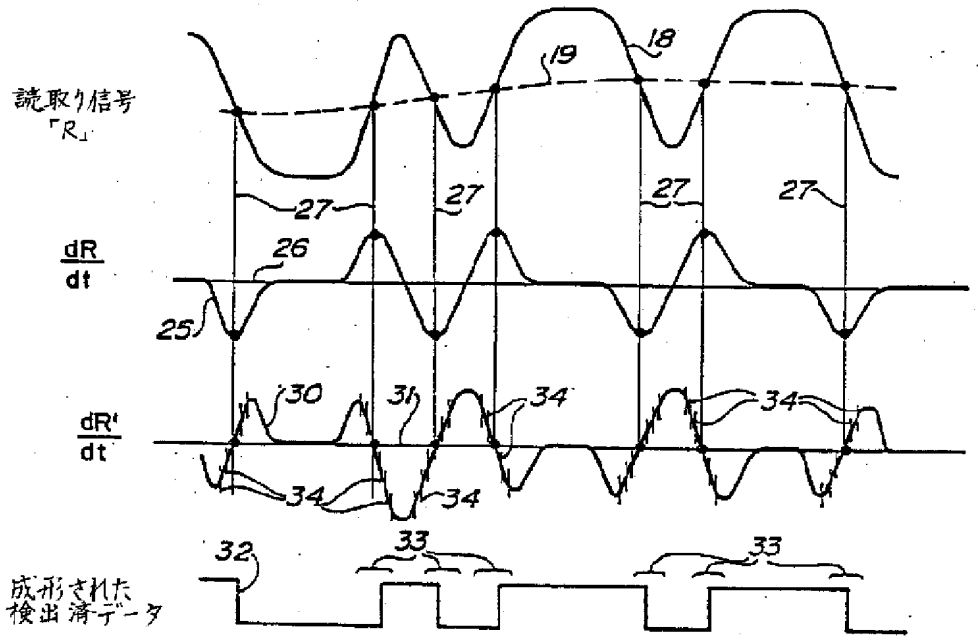
【図３】



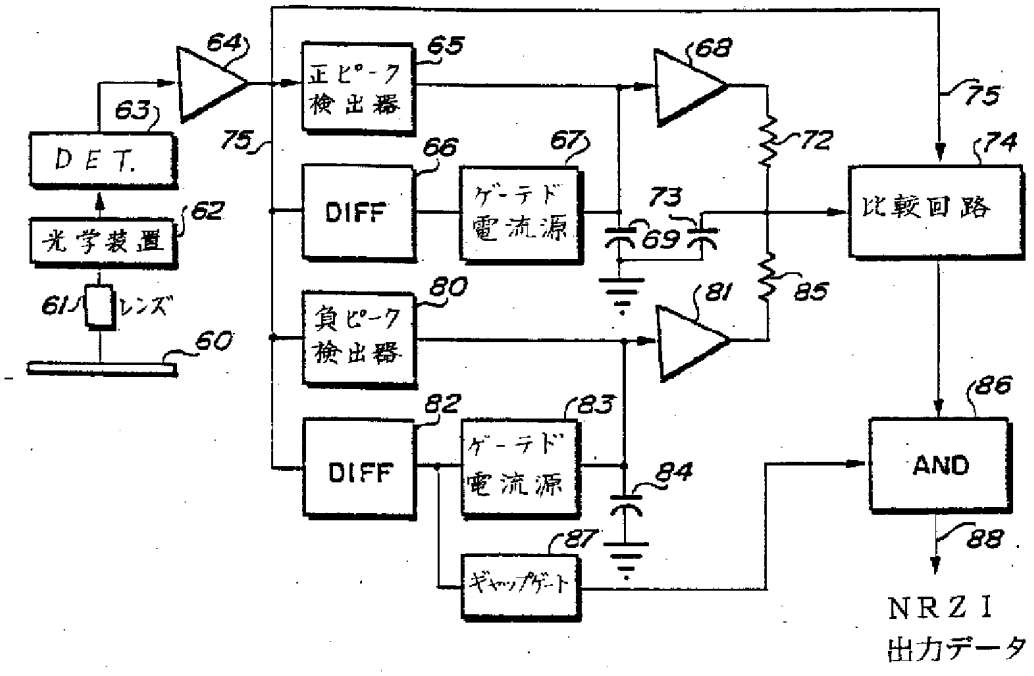
【図４】



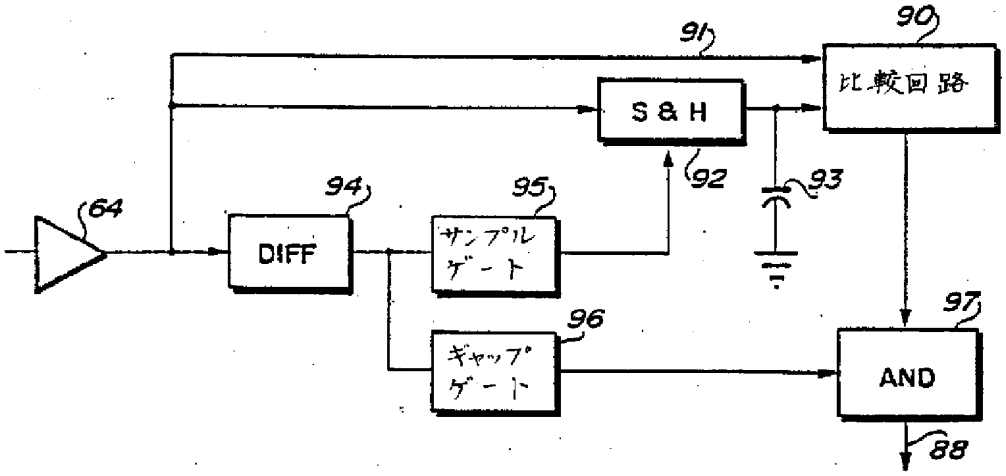
【図2】


読取り信号
「R」
dR/dt
dR'/dt
成形された
検出済データ
18
19
25
26
27
30
31
32
33
34

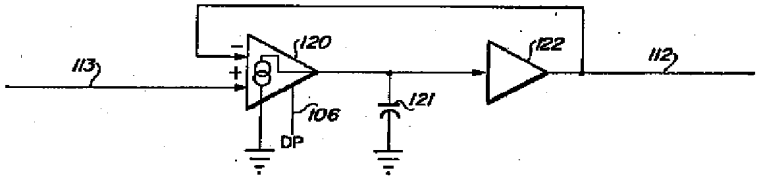
【図5】


DET.
光学装置
レンズ
正ピーク
検出器
負ピーク
検出器
DIFF
DIFF
ゲーテド
電流源
ゲーテド
電流源
ギャップゲート
比較回路
AND
NRZI
出力データ
60
61
62
63
64
65
66
67
68
69
72
73
74
75
80
81
82
83
84
85
86
87
88

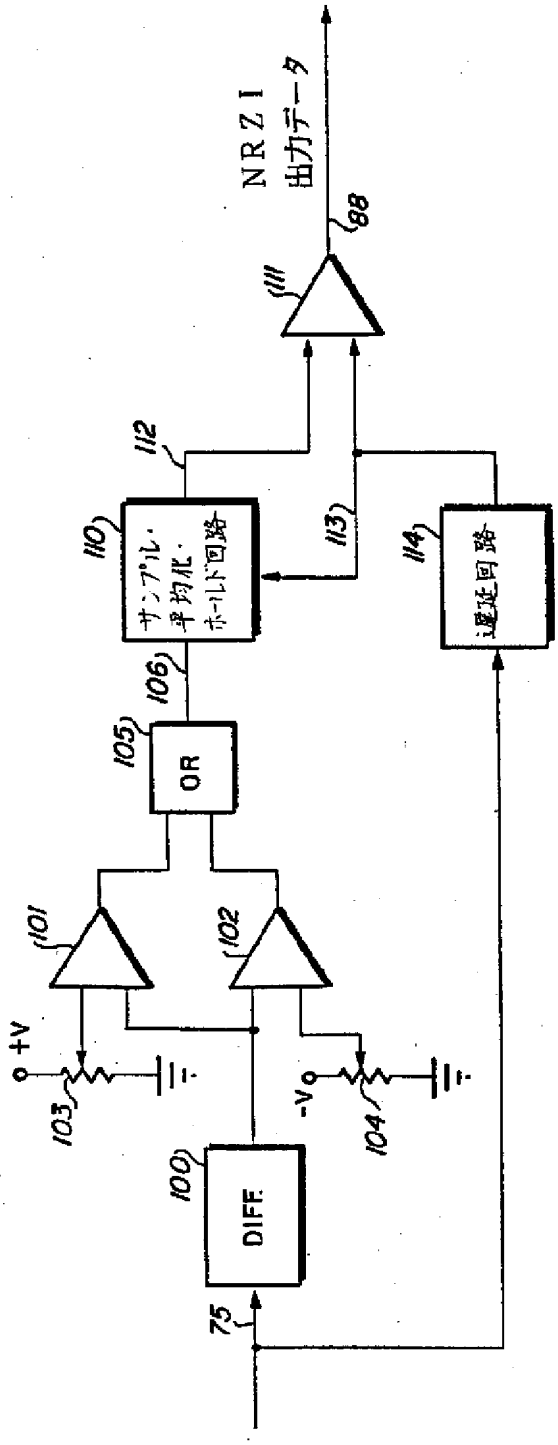
【図６】


91
90
比較回路
S & H
92
93
94
95
64
DIFF
サンプル
ゲート
96
97
ギャップ
ゲート
AND
88

【図８】


113
120
122
112
106
121
DP

【図7】


NRZI
出力データ
88
111
112
110
サンプル・
平均化・
ホールド回路
113
114
遅延回路
106
105
OR
101
102
+V
-V
103
104
100
DIFF
75

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